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APPLICATION

FOR

UNITED STATES LETTERS PATENT

Be it known that I, Frank H. Peters residing at 1170 Wilhelmina Way; San Jose, CA 95120 and a citizen of Canada, have invented new and useful improvements in:

ELECTRICAL ISOLATION OF ELECTRO-OPTIC COMPONENTS IN PHOTONIC INTEGRATED CIRCUITS (PICs)

of which the following is the specification.

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ELECTRICAL ISOLATION OF ELECTRO-OPTIC COMPONENTS IN PHOTONIC INTEGRATED CIRCUITS (PICs)

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REFERENCE TO RELATED APPLICATION

[0001] This application is a continuation of patent application, Serial No. 10/283,476, filed October 30, 2002, which application claims priority to U.S. provisional application, Serial No. 60/402,801, filed June 21, 2002, which applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] This invention relates generally to photonic integrated circuits (PICs), including electro-absorption modulators/lasers (EMLs), and more particularly to electrical isolation of electro-optical components in such circuits.

Description of the Related Art

[0003] In photonic integrated circuits or PICs, two or more active or electro-optical components as well as possibly at least one passive optical component are generally integrated on a single semiconductor or other type of chip. A well known example of this kind of PIC chip is an EML (Electro-absorption Modulator/Laser) where, for example, a distributed feedback (DFB) laser is integrated with an electro-optical modulator such as illustrated, for example, in U.S. patent 6,148,017, employing the InGaAsP/InP regime. There are many such examples of EMLs in the art and this just one recent example of this type of device. In order that there is no electrical interference between the operation of these integrated electro-optical components, an electrical isolation region (which is shown at reference number 5 in the above mentioned patent), which is usually an isolation trench, is generally deployed between such optical components. The trench usually extends down into the bulk of the PIC chip as far as the upper confinement layer, for example, above the active region of the PIC chip. However, it is desirable not to extend such a trench too far into the chip so as to perturb the optical mode propagating in the active region of the device as well as cause significant backward reflections of the optical mode since such a trench can function as a partial mirror to the propagating mode.

[0004] These types of EMLs suffer from lack of good electrical isolation between the optical modulator and the DFB laser because the trench is still not deep enough to provide good avoidance of electrical interference, particularly in the separation of the operation of the DFB laser from the electrical modulation of the optical modulator. In particular, parasitic current paths still exist between these electro-optical components. For example, in EMLs, a parasitic path will exist below the isolation trench between the DFB laser and the electro-optical modulator such that the DFB laser will experience fluctuation changes in its drive current via the fluctuations of the parasitic current established between the laser and modulator. This modulated parasitic current perturbs the operation of the DFB laser. As indicated above, generally the isolation trench cannot be made deeper into the PIC chip in an attempt to further electrically isolate the DFB laser from the optical modulator without affecting the properties of the propagating optical mode.

OBJECTS OF THE INVENTION

[0005] It an object of the present invention to overcome the aforementioned problems.

[0006] It is a further object of this invention to provide for electrical isolation particularly between electro-optical components in a PIC, such as an EML without affecting the propagating optical mode in the PIC.

SUMMARY OF THE INVENTION

[0007] According to this invention, a method is directed to forming an electrical isolation region is formed between adjacently disposed electro-optical components integrated in a monolithic semiconductor photonic chip, such as an EML or PIC chip, wherein a bias, V_C, is applied to the isolation region so that any parasitic current path developed between adjacently disposed electro-optical components, now separated by the isolation region, is established through the electrical isolation region and clamped to the bias, V_C. The applied bias, V_C, may be a positive bias, a negative bias, or a zero or a ground bias. While EMLs have been exemplified herein, other electro-optical devices integrated on a semiconductor chip may also be benefited by the isolation region utilized in this invention, such as, for example, a photodetector (PIN) photodiode or avalanche photodiode (APD)), a semiconductor optical amplifier (SOA) or a gain clamped semiconductor amplifier (GCSOA), also referred to as a semiconductor laser amplifier, as well as a semiconductor electro-absorption modulator (EAM), Mach-Zehnder modulator (MZM), DFB laser or DBR laser.

[0008] In the method of establishing electrical isolation regions, they may be, for example, formed by spatial current blocking regions at adjacent sides of the electrical isolations region transverse to a direction of light propagation through electro-optic components and/or optical passive components formed in the PIC chip, or said another way, between each electrical isolation region and an adjacent optical component which all integrated into the PIC chip. The spatial current blocking regions sandwiching the electrical isolation region is coupled to bias, V_C, for capturing any parasitic current flow between the electro-optic components or optical passive components in the PIC chip. The preferred embodiment for spatial current blocking regions herein is spatially disposed trenches between which the electrical, biased isolation region of this invention is achieved. However, it is within the scope of this invention to provide such isolation regions utilizing means other than trenches, such as by forming insulating regions via doping, e.g., Fe doping, or via ion implant, e. g., H^+ implantation, or other processes or structures that would form such an electrical isolation region.

[0009] While general mention here is made of active or electro-optical components and their electrical isolation from one another, it should be understood that the isolation regions of this invention may also be utilized between active and passive optical components formed in a PIC chip, such as between PIN photodetectors or electro-optical modulators and an optical combiner (multiplexer), such as an arrayed waveguide grating (AWG), where the refractive index of the latter can be affected by induced parasitic current paths established from such active devices to the passive device changing slightly its waveguide properties due a to slight change in refractive index in at least a portion of the passive device due to such parasitic current flow.

[0010] Other objects and attainments together with a fuller understanding of the invention will become apparent and appreciated by referring to the following description and claims taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] In the drawings wherein like reference symbols refer to like parts:

[0012] Fig. 1 is a schematic plan view of an example of a photonic integrated circuit (PIC).

[0013] Fig. 2 is a schematic view of a more detail of the PIC shown in Fig. 1.

[0014] Fig. 3 is schematic plan view of a PIC of the type shown in Fig. 1 utilizing the electrical isolation regions of this invention between adjacently disposed optical components integrated in the PIC chip.

[0015] Fig. 4 is a schematic cross-sectional view along the line 4-4 of Fig. 3.

[0016] Fig. 5 is a schematic cross-sectional view taken along either of the lines 5-5 of Fig. 4.

[0017] Fig. 6 is a schematic cross-sectional view taken along the line 6-6 of Fig. 4.

[0018] Fig. 7 is a perspective view of a portion of the PIC shown in Figs. 3-6.

[0019] Fig. 8 is an electrical circuit representation of an EML as known in the art having at least one parasitic current path.

[0020] Fig. 9 is an electrical circuit representation of an EML illustrating a parasitic current path to an electrical isolation region of this invention rendering such a current path negligible relative to the functionality of adjacently disposed optical components integrated in the same chip.

DETAILED DESCRIPTION OF THE INVENTION

[0021] Reference is now made to the details of an embodiment of a type of photonic integrated circuit (PIC) that may be utilized in connection with this invention. It should be understood that while a multi-component PIC devices are illustrated in connection with this invention, any optical device that includes adjacently integrated optical components where at least one of the components is an active device, i.e., an electro-optical operated component, may utilize this invention.

[0022] Referring now to Fig. 1, the illustrated PIC device comprises a transmitter photonic integrated circuit or TxPIC 10. The architecture of TxPIC 10 is further detailed as to structure, operation and functionality in previously filed patent applications, Serial Nos. 10/267,331; 10/267,330; 10/267,346; and 10/267,304, all filed October 8, 2002, which applications are all incorporated herein by reference. While the first three referenced applications all deal with TxPICs, the last mentioned application, Serial No. 10/267,304, deals with receiver photonic integrated circuits (RxPICs) to which this invention can also be applied, for example, relative to electrical isolation of the photodetectors formed in a RxPIC chip from other active (e.g., SOAs) or passive (e.g. AWG) components integrated in the same PIC chip.

[0023] In Fig. 1, TxPIC 10 comprises an InP-based semiconductor chip which includes integrated optical and electro-optic components formed as integrated electro-optic circuit. Chip 10 comprises a plurality of aligned DFB lasers 14 each having a different operating wavelength within a standardized wavelength grid, such as the ITU grid. Laser 14 can also be a distributed feedback (DFB) laser. There are twelve such lasers and signal channels shown in Fig. 1. However, there may be any number of such channels on-chip, for example, ranging from 4 to 40 channels. Some of these signal channels may be redundant channels for use in place of inoperative lasers or modulators or EMLs. These DFB lasers 14 are wavelength stabilized as set forth in the above identified provisional applications. Each of the twelve channels in chip 10 also includes an optical modulator 16 to modulate the light output of a respective CW operated DFB laser 14. Chip 10 may also include an array of PIN photodiodes 12 to monitor the power and wavelength of each DFB laser 14. Also, an array of PIN photodiodes 18, respectively following each modulator 16, may be utilized to monitor the power, chirp and extinsion ratio of modulator 16. These photodetectors 12 and 18 are optional in TxPIC 10 so that TxPIC 10 may be, at a minimum, an array of DFB lasers 14 and modulators 16 and an optical combiner 20 of some type. The modulators 16 may be, for example, electro-absorption modulators (EAMs) or Mach-Zehnder modulators (MZMs). The outputs 31 from PIN photodetectors 18 are optical waveguides formed in chip 10, and are formed in fan arrangement from PINs 18 to the input of an optical combiner 20 which is shown here as an arrayed waveguide grating (AWG) comprising an input slab 22, a plurality of grating arms 26 of predetermined increasing length and an output slab 24 as known in the art. Optical combiner 20 may also be echelle grating, a multi-mode interference coupler, a star type coupler, or a slab or free space coupler. AWG 20 combines the modulated signals on waveguides 31 into a WDM signal that is provided on one of the vernier output waveguides 27 formed in chip 10 from output slab 24 for taking the multiplexed channel signals off-chip. The waveguide 27 having the best signal spectrum from AWG 20 is chosen as the output for launching the WDM signal onto an optical fiber.

[0024] Fig. 2 shows additional details of TxPIC chip 10 of Fig. 1. To be noted is that chip 10 has twelve signal channels and has a chip size that is fairly small comprising, for example, 3.5 mm by 4.5 mm. DFB lasers 14(1)...14(12) are set on center-to-center spacing, for example, of about 250 μm. Also shown is the DC biasing for laser monitoring PIN photodiodes 12(1)...12(N), DFB lasers 14(1)...14(12), optical modulators 16(1)...16(12) and modulator monitoring PIN photodiodes 18(1)...18(12). On-chip heaters 15(1)...15(12), which may be strip heaters, for example, are provided for each laser and independently operated to maintain

the peak operating wavelength of each laser to its proscribed wavelength on the standardized grid. Also, a heater 21 may be provided to control the wavelength grid of AWG 20 in conjunction with the control of the individual operating wavelength of DFB lasers 14 via heaters 15(1)...15(12). This wavelength grid control is explained in further detail in the above referenced provisional applications. Lastly, each of the modulators 16 has a coaxial or coplanar electrode arrangement 17(1)...17(12) to provide to each modulator 16 with an electrically modulated signal for modulating the cw light provided from DFB lasers 14, i.e., to accomplish EO signal conversion, signal multiplexing at AWG 20 and launching the multiplexed signal via output waveguide 27 onto optical fiber link 28.

[0025] Reference is now made to Fig. 3 illustrating a plan view of TxPIC 10 utilizing isolation regions 32 of this invention. PIC chip 10 in Fig. 3 is the same as that shown in Figs. 1 and 2 except that only one optical signal channel is shown for purposes of simplicity of explanation. The electrical isolation regions 32 are formed by spatial current blocking regions 30 formed at adjacent sides of electrical isolations regions 32 transverse to a direction of light propagation through the optical components, or between the electrical isolation regions and adjacent optical components. Spatial current blocking regions 30 may be comprised of a pair of: (1) spatially disposed trenches or (2) ion implanted regions or (3)high resistance implanted regions. In the preferred embodiment, regions 32 are shown as a pair of spatially disposed trenches 30.

[0026] As shown in Figs. 4-7, TxPIC 10 comprises an InP substrate 40, either semiconductive (n-doped) or insulating (Fe-doped), upon which is epitaxially ("epi") deposited, employing MOCVD, an InP buffer layer (not shown) followed by a n-doped InP layer 42 and a quaternary grating layer 44 of AlInGaAs or InGaAsP. These quaternary layers are referred to herein collectively as a "Q" layer or layers. A selective etch is then performed to form grating region 46 in the DFB portion of PIC 10. After formation of grating 46, epi growth is continued with the deposit of n-InP layer 48, Q active/waveguide region 52 (which generally comprises multiple quantum wells and barriers), nonintentionally doped (NID) InP layer 52, Q stop etch layer 54, cladding layer 56 of p-InP, p^+-InP layer 58 and contact layer p^{++}-InGaAs. As shown best in Figs. 5 and 6, a selective etch is performed longitudinal between adjacent optical pathways constituting signal channels, such as the twelve signal channels illustrated in PIC 10 of Fig. 2, where each channel comprises a DFB laser 14, a MOD 16, PIN 18 and an optical combiner 20, such as an AWG , star or slab coupler. The selective etch is performed down to the stop etch Q layer 54. It is within the scope of this description that other stop etch

layers, other than a Q layer, may be utilized to perform the stop etch function. For example, the stop etch layer may also be NID AlInAs, or InAlGaAsP.

[0027] As illustrated in Figs. 5 and 6, the resulting etch forms a ridge waveguide structure 61 provides sufficient mode guiding while permitting expansion of the propagating mode 62 into ridge waveguide 61 which correspondingly permits an increase in the light intensity of the mode. In other words, the propagating mode is less confined in the waveguide structure which includes Q layers 44 and 50. This is important from the standpoint of having sufficient on-chip power in the modulated channel signals that are optically combined and presented at the output of the InP chip 10 without any requirement of on-chip amplification, such as via integrated, on-chip semiconductor optical amplifiers (SOAs) which require the supply of additional power to TxPIC 10 for their operation. This would significantly impact the power budget of chip 10. Also, alternatively, the ridge waveguide may include a Q layer (not shown) which is formed within the ridge waveguide to provide a rib-loaded waveguide which permits the propagating mode to expand even more into the ridge waveguide thereby permitting a further increase in optical mode intensity.

[0028] Returning now to Figs. 4 and 7, in order to reduce or otherwise eliminate parasitic or leakage currents that naturally forms between adjacent optical components, particularly with respect to active or electro-optical components, such as DFB lasers 14, MODs or EAMs 16 and PINs 18, isolation regions 32 are formed between these optical components 14, 16, 18 and 20. As an example, these isolators or isolation regions 32 may be about X = 20 μm in length, although they may also be smaller or larger in size. The preferred approach is to render them as small as possible in length and still perform the function of clamping parasitic or leakage currents that developed between adjacent optical components to a bias voltage point or ground. The reason is to conserve as much as possible room or real estate on PIC chip 10. Isolation regions 32 thus perform two important functions. First, they electrically isolate adjacent optical components by clamping parasitic or leakage flows to a voltage or ground. Second, they help to render the resistance in the PIC structural layers sufficiently large so that these leakage currents are at least reduced to the microampere range. For example, layers 52, 54 and 56 may be ion implanted in areas below isolation regions 32 to increase resistivity.

[0029] Isolation regions 32 are formed by forming spatial current blocking regions 30 via performing a selective etch to provide dual isolation trenches 30 between which is defined isolation region 32, as shown in Figs. 3 and 4. These trenches are formed at an angle, i.e., transversely, relative the longitudinal axis of the light propagation path through components

14, 16 and 18, such as, for example, angled at 7° from a line perpendicular to the longitudinal axis of light propagation, in order that any reflections of the propagating optical mode are reflected out of the light propagation path. Also, as best seen in Figs. 4 and 7, the depth of trenches 30 is through layers 58 and 60 so as not made too deep so as to have a significant effect on the propagation of the mode 62. Also, as best seen in Fig. 7, the selective etch to form the ridge waveguide extends through layers 56, 58 and 60 to etch stop layer 54. However, portions of the etch stop layer between adjacent light propagation paths via the ridge waveguides may also be removed as shown in Fig. 7, which renders layer 54 as part of the ridge waveguide 61.

[0030] In order to provide some passivation, trenches 30 as well as the surface of PIC chip 10 may be covered with a layer of dielectric material, such as BCB or polyimide. As previously indicated, beside the deployment of etched trenches 30, spatial current blocking regions 30, comprising etched trenches 30,can be made of high resistance by Fe doping into unetched spatial current blocking regions 30 or performing an ion implant into unetched spatial current blocking regions 30 such as via an H^+ implant.

[0031] It should be understood that a balance is achieved between the parameters of the height of the ridge waveguide 61, the depth of the trenches 30 and the control of bulk resistance in regions below trenches 30. It is desirable, for example, to increase the height of ridge waveguide 61 but not so high that the propagating mode experiences significant reflections due to the walls of trenches 30. Thus, the trenches 30 should not be so deep as to significantly affect the propagating mode but it is also desirable to make trenches 30 sufficiently deep to better electrically isolate adjacent optical components where the propagating mode experiences only negligible optical reflections. One additional parameter in this balance of parameters is to also enhance the resistive nature of the of areas below isolation regions 32, such as, for example, p-InP layer 56 and/or Q layer 54 where the doping concentration in layer 56, in particular, is decreased or an ion implant is made into the areas of layers 54 and 56 below isolation regions 32 during the growth process to render the bulk resistance of these areas higher, as previously alluded to above concerning the two functions pertaining to isolation regions 32.

[0032] Reference is now made to Figs 8 and 9 to explain how, from an electrical point of view, the isolation regions 32 perform their functions. It should be realized that voltage biases shown in these figures is merely representative of one set of conditions as other such voltage biases, either higher or lower, may be desired or necessary depending upon the operating

parameters of the particular electro-optical components and the bulk resistance of the PIC structure. As shown in the case of Fig. 8 where there is a single isolation trench, as discussed previously in connection with the prior art, or there is no isolation, there is established a current path to operate DFB laser 14A with current flow, I_1, from a positive bias point 64 to reference or ground 65 (R_L represents the resistance in the path including of DFB 14A), and a current path to operate MOD 16A with a current flow, I_3, from reference or ground 65 to a negative bias point 66 (R_M represents the resistance in the path including of MOD 16A). Also, as an example, a parasitic path is established from positive bias point 64 to negative bias point 66 with a parasitic current flow, I_2, in the semiconductor bulk between DFB laser 14A and MOD 16A which is represented by a bulk resistance of R_P. As MOD 16A is modulated via current, I_3, the level of current flow, I_2, will correspondingly fluctuate to bias point 66. Also, correspondingly, the current flow, I_1, will vary in accordance with changes in current flow, I_2. Changes in the current flow to DFB laser 14A is not desirable because changes in the applied current create corresponding changes in the desired or predetermined operational wavelength of the laser via refractive index changes in the laser due to current changes across the diode. However, in the case of the deployment of the isolation regions 32 of the present invention, as shown in Fig. 9, the path for parasitic current flow, I_2, is changed and divided into two separate paths such that the parasitic current flow, I_{2A}, relative to DFB 14, is from positive bias point 62 to reference or ground 65, via the PIC bulk resistance R_{P1}, while the parasitic current, I_{2B}, relative to MOD 16, is from reference or ground 65 to negative bias point 66, via the PIC bulk resistance R_{P2}. The modulated current will also correspondingly cause reflection of parasitic current, I_{2B}. To be noted is that parasitic current flow, I_{2A}, from DFB laser 14 since this current is clamped to V_C, will not vary, and the fluctuation of current flow, I_{2B}, will have negligible effect on the desired steady state (CW) condition of current flow, I_1. Also, the bulk resistances, R_{P1} and R_{P2}, can also be designed to enhance their resistance levels, as previously discussed, so that current flows I_{2A} and I_{2B} are at least reduced to the microampere range.

[0033] While the invention has been described in conjunction with several specific embodiments, it is evident to those skilled in the art that many further alternatives, modifications and variations will be apparent in light of the foregoing description. As previously indicated, for example, this invention may be applied to any PIC chip or associated optical component including for example, EMLs, RxPIC chips or any other chip that contains optical or electro-optical adjacently disposed components or elements. In connection with components such as photodetectors that follow EAMs on a PIC, it should be noted that are

instances that these photodetecting elements may also, themselves, be modulated for purposes of tagging or otherwise identifying the respective outputs of the several DFB lasers14 as well as performing a monitoring function for the electro-optical characteristics of MODs 16. In such cases, the electrical isolation of fluctuating parasitic currents from either the EAMs or the photodetector elements due to their modulation can be accomplished by the use of clamping isolation regions 32. Thus, the invention described herein is intended to embrace all such alternatives, modifications, applications and variations as may fall within the spirit and scope of the appended claims.